Remarks/ Arguments

In response to the Office Action mailed September 22, 2004, Applicants respectfully request that the Examiner reconsider the objections to the specification and the claims. Applicants note with appreciation the allowability of objected – to Claims 2 and 5.

Claims 1 - 6 remain.

Claims 1, 3 – 4, and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Browen* (U.S. Patent 6,327,545) (hereinafter "the *Browen* reference"), in further view of *Shibuya et al.* (U.S. Patent Re. 34,295) (hereinafter "the *Shibuya* reference"). Applicants respectfully traverse these rejections.

Specifically, the *Browen* and *Shibuya* references, taken alone or in combination, do not teach or suggest stepping a current to an integrated circuit from a reference level by a selected current step representing an error detected at a selected test node. Furthermore, the *Browen* and *Shibuya* references, taken alone or in combination, do not recognize the advantages of applying the present inventive principles, including the capability of transmitting a substantial amount of test information with a minimum number of pins.

The *Browen* reference discloses a system primarily suitable for testing circuit boards, and which includes measurement hardware 106 and a fault analysis subsystem 108, as shown in Figure 1. The *Browen* reference does not suggest that either measurement hardware 106 or fault analysis subsystem 108 represents detected errors utilizing current stepping.

Similarly, the *Shibuya* reference does not teach or suggest stepping a current to an integrated circuit from a reference level by a selected current step representing an error detected at a selected test node. In particular, Figure 1 of the *Shibuya* reference only discloses a digital to analog converter (DAC) system including an integrated circuit 14, external switches 18 and 19, external current sources 20 and 21, and an external

operational amplifier (opamp) 24. Generally, the digital input data is loaded into a pair of counters 10 and 11. Counters 10 and 11 then count from the value of the input data to a predetermined value, at which time pulse signals are generated. These pulse signals switch constant currents from current sources 20 and 21 through switches 18 and 19 to the integration capacitor 13 of opamp 24. The result is an analog signal at the output of opamp 24.

Since the *Browen* and *Shibuya* references do not teach or suggest, either alone or in combination, the feature stepping a current to an integrated circuit from a reference level by a selected current step representing an error detected at a selected test node, Applicants respectfully submit that the rejections of Claims 1, 3 – 4, and 6 under 35 U.S.C. § 103(a) should be withdrawn.

No new matter has been added; the claims have been merely amended to more particularly claim the subject matter Applicants believe is inventive. Applicants respectfully submit that the Claims as they now stand are patentably distinct over the art cited during the prosecution thereof.

Applicant respectfully requests a First Month Extension of Time to File this Response. Enclosed with this paper is Form PTO/SB/22 with Extension Fees in the amount of $120.00.

With the addition of no new claims, no additional filing fees are due. However, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 20-0821 of Thompson & Knight LLP.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (214) 969 - 1749.

Respectfully submitted,
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